

Self-Alternating Mode for Transistors Supported by Specialized Quartz Material to Enable Conventional CPUs to be Optimized for High-Floating-Point or Artificial Intelligence Applications on As-Need-Be Basis

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Introduction

Various computational applications have created niche markets for application-specific processors (the two primary examples being high-FPU and AI applications) which are physically optimized to perform those tasks. In the not-too-distant future, given the impressive advancement of thought-to-speech translation (to cite merely one example,) there may be a market for integrated, compact processors capable of efficiently handling conventional computational tasks, AI-type tasks, as well as high-FPU tasks. If one wishes to have a conversation with a person in real-time who speaks a different language without needing to speak into a voice-to-text translator, thought-to-translated speech would be the logical solution. While there are surely many other such examples of future applications calling for all three modes of function, the high cost of ASICs has limited their availability to those with substantial financial resources and limited their implementation to workstation and mainframe-scale operation.

Achieving feats such as thought-to-speech, thought-to-text and thought-to-foreign language text or speech would require AI-optimized function within the processor of a smart phone in order to recognize the EM signature of key neural patterns and match them to specific words (and more importantly, concepts) in the speaker's native language but would, furthermore, require translation into a given foreign language and would most likely also require a high-FPU architecture for some portions of such a process.

This publication will describe an approach which would enable a conventional CPU with certain added features to be controllably optimized for performing these other tasks on an as-need-be basis. If demonstrated to be practical, the following approach will reduce the cost of application-specific processing while providing the flexibility which would be needed in order to optimize a CPU for unforeseeable future applications. Everything from data compression to random number generation would also likely benefit from the following CPU design modifications.

Abstract

In the case of high-FPU applications, the ability to rapidly switch a single transistor between the 'on' and 'off' state is the most crucial aspect of operation. Ordinarily, the switching of a transistor is achieved by sending an electrical impulse through a series of wires toward those transistors. In a conventional CPU, these impulses must pass through a series of switches, junctions, gates,

bifurcated pathways etc. in order to arrive at a given destination. In the case of a high-FPU-optimized architecture such as that of a graphics card, the number of transistors is increased and parallelization is increased so that pulses may take a more direct route to transistors. Meta-analysis of computational outputs is de-emphasized and sequential alternation is emphasized.

In the case of AI applications, a different mode of operation is required. Rather than needing to rapidly cycle through every possible combination via massive parallelization, AI-optimized processors are predicated upon the introduction of subtle changes to values in a system with maximal speed and randomness. The more that machine-learning can be hardware-accelerated, the more efficient AI software may become. As machine-learning (ML;) as it is currently understood; is supported by the introduction of chaotic variation in matrices, the ability to chaotically alternate transistor charge states in complex computational systems would be supportive of AI applications.

Toward both of the aforementioned ends, the use of a quartz or quartz-like pulsation mechanism which receives a steady supply of energy but which pulses at a predictable frequency could be used in order to alternate transistor charge states locally rather than non-locally via wires. These Local Charge State Alternating Crystals (LCSACs) would be powered by an efficient induction mechanism (ideally the herringbone inducer ibid. 17 February 2024) which could be either powered or not powered depending upon whether hardware acceleration of applications-specific tasks are required.

Physical portions of a CPU could be logically partitioned i.e. *treated differently by the overall logic of the CPU* when these specialized modes are engaged so that the CPU knows to expect irregular values for transistor charge in those sections and does not attempt to inappropriately overwrite those values although it would continue to read those values. When high-FPU tasks are called for, a section with crystals optimized for running through all possible binary combinations sequentially (e.g. each transistor in a series would have a crystal the firing time of which is half as frequent as the last by dint of its physical characteristics rather than a conventional switch.) When AI-optimization is called for, a different section of processor in which conventional transistors are collocated with LCSACs wherein the firing time of the crystals is randomly varied by physical design and in which active and inactive LCSACs are also varied programmatically. Large numbers of low-amperage induction power transmitters would be employed and switched randomly on or off in order to introduce variations in the charge states of transistors when such a processor is functioning in the ML mode. In this way, the ML application which calls for the insertion of many random values into computations at, essentially, midway through the computational process, would be enhanced as these values could be changed more rapidly and more directly when the source of charge is immediately collocated with the transistor and when multiple physical gates do not have to be accessed in order to change a charge state. The ordinary physical wiring of a CPU, the timing of the LCSACs and the on or off state of the power transmitter would all act as randomizers of charge state in this mode of function.

As the ML application does not require precision and, in fact, thrives on chaos, this is one case in which making random changes to the charge state of transistors would actually be helpful.

Conclusion

Primary challenges would include identifying crystalline compounds with sufficient pulsation timings to be useful for GHz-regime operation manufactured with sufficient precision so as to ensure that alternation timing falls within expected parameters. These pulse timings would most easily be controlled through variation in crystal size, as is the case with quartz. The crystals should be lattice-form with the smallest (and fastest) being composed of four atoms and with timing being halved for each doubling in size. To ensure proper timing, induction should be used to power these LSCACs in order to mitigate irregularities in pulse rate caused by multiple crystals deriving their charge from the same circuit.

This overall approach could be used not only to allow for conventional CPUs to optimized their own mode of function upon demand but in order to produce qualitatively improved dedicated ASICs, as well.